Means for Forming SOI

Background and Summary of the Invention

The present invention relates to integrated circuit structures and fabrication methods, and particularly to formation of silicon-on-insulator wafers.

Background

Silicon on insulator (SOI) devices are important additions to IC technology for many reasons, allowing isolation of devices, low power, and low voltage technologies, as well as reducing parasitic capacitance and the accompanying latch-up. Many technologies have been developed for the fabrication of SOI devices, including separation by implanted oxygen and bonded wafers.

Porous silicon has also been used to form SOI by bonding wafers and later removing the porous layer, leaving an epi layer with an oxide (which was originally grown on the epi by conventional means, and sandwiched by another wafer). The porous silicon in such a process is used as an etch-stop for the BOX.

Means for Forming SOI

The present application discloses an innovative way to make a SOI wafer. In the preferred embodiment, a wafer surface is anodized to form a porous silicon layer at the surface, which is sealed, preferably by heating it in an H2 ambient, after cleaning to remove any surface oxide. A thin silicon film is then formed by standard deposition techniques. The porous silicon is then implanted with a low dose of

oxygen, followed by a high temperature anneal. The oxygen implant forms the buried oxide layer. Additional epi layers may be formed on the layer of monocrystalline silicon on the surface.

Advantages of the disclosed methods and structures, in various embodiments, can include one or more of the following:

- porosity of silicon prevents clumping (formation of clusters rather than a uniform layer) of SiO2 with low dose;
- relatively thick dielectric layer for given dose size;
- aids in planarity of SPIMOX;
- porous silicon readily oxidizes, allowing sharp definition of oxide layer.

Brief Description of the Drawings

The disclosed inventions will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by reference, wherein:

Figure 1 shows a flow chart of the preferred embodiment.

Figures 2a-2c show the formation of the SOI structure at different process steps.

Detailed Description of the Preferred Embodiments

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood that this class of embodiments provides only a few examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

Figure 1 shows a series of steps for practicing the preferred embodiment. First a layer of porous silicon is formed by anodizing a boron doped (0.001-0.02 ohm-cm) silicon wafer (**step 1**). In the preferred embodiment, a HF+C2H5OH combination is used. The depth of the porous silicon can be controlled by timing or by limiting the depth of the boron doping. Thicknesses in the range of nanometers to microns can be obtained. Next the porous silicon surface is cleaned by diluted HF and then by deionized water in order to remove only the wafer surface oxide. Next an epitaxial layer is grown on the porous silicon surface (**step 2**). The porous layer is then implanted with oxygen using a plasma oxygen implant or other oxygen implantation methods (**step 3**).

The present application teaches that the porous silicon can be covered with a layer of epi and converted to an oxide by introducing oxygen into the porous silicon. At least a thin layer of epi should be formed prior to oxidation of the porous silicon. Additional epi layers may be added later.

Figures 2a-2c show the innovative formation of the SOI during various fabrication steps. **Figure 2a** shows the wafer substrate **202** after anodizing. The top surface of the wafer exhibits cracks extending into the depth of the surface resulting from the anodizing process. This area of the wafer comprises the porous silicon **204**. The porous silicon 204 is treated by a prebake to fill up some of the surface pores with silicon atoms that migrate toward the pores in order to reduce the surface energy of the wafer.

Figure 2b shows the wafer 202 and porous silicon 204 covered by a thin layer of epi **206**. The quality of the epi 206 depends on the surface pore filling during the sealing bake of the wafer in a nitrogen, hydrogen, or inert ambient. A thin layer of epi used as a seal is required to give a starting point for later epi growth.

Figure 2c shows the wafer 202 and porous silicon 204 with the epi layer 206. Oxygen **208** has been implanted into the porous silicon through the epi layer. Note that the oxygen implantation could be performed before the final epi formation. Oxygen doses on the order of 10^17 to 10^18 oxygen ions per cm^2 are used in the preferred embodiment. Though 10^18 is a relatively heavy dose, this may be done cheaply with plasma implantation into the BOX. High temperatures are used during oxidation, on the order of 1000 C for about 30 minutes.

Another possible process flow grows the epi layer over the porous silicon before the oxygen is implanted. As another variation, a standard but low dose oxygen implant can be used instead of using SPIMOX.

The porous silicon surface, after it has been formed but before

oxygen has been implanted or epi has been grown, can be sealed in an inert ambient, a nitrogen ambient, or a hydrogen ambient, depending on the process.

According to a disclosed class of innovative embodiments, there is provided: A method of forming a semiconductor-on-insulator structure, comprising the steps of: a) forming a structure having porous semiconductor material at a first surface thereof; b) introducing an oxidizing species into said porous semiconductor material; and, either before or after step b), c) forming an epitaxial semiconductor layer on said porous semiconductor material, and reacting said oxidizing species with said porous semiconductor material to form a buried dielectric layer beneath said epitaxial layer.

According to another disclosed class of innovative embodiments, there is provided: A method of forming a semiconductor-on-insulator structure, comprising the steps of: a) anodizing a silicon wafer to form porous silicon; b) introducing oxygen into said porous silicon; and, either before or after step b), c) forming a semiconductor layer on said porous silicon, and reacting said oxygen with said porous semiconductor material to form a buried oxide layer.

According to another disclosed class of innovative embodiments, there is provided: A method of forming a semiconductor-on-insulator structure, comprising the steps of: a) partially anodizing a silicon wafer to form porous silicon; and thereafter b) forming an epitaxial semiconductor layer on said porous silicon; and thereafter c) introducing oxygen into said porous silicon, and reacting said oxygen with said porous silicon to form a buried oxide layer.

Modifications and Variations

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and accordingly the scope of patented subject matter is not limited by any of the specific exemplary teachings given, but is only defined by the issued claims.

Impurities can be incorporated into the BOX to alter the characteristics of the device.

It is also contemplated that Si/Ge layers can be grown over a porous-silicon-derived oxide layer.

Also, in alternative embodiments the porous silicon does not have to be completely oxidized.

In another class of alternative embodiments, it is contemplated that the oxidizing species does not have to be derived from molecular oxygen, but can be derived from oxidizing gasses such as O3 or N2O.

In another class of alternative embodiments, it is contemplated that other elements besides oxygen can be used for the self-segregating reaction which forms the buried layer.

The teachings above are not necessarily strictly limited to silicon. In alternative embodiments, it is contemplated that these teachings can also be applied to structures and methods using other semiconductors, such as silicon/germanium and related alloys, gallium arsenide and related compounds and alloys, indium phosphide and related compounds, and other semiconductors, including layered heterogeneous structures.

Additional general background, which help to show the knowl-

edge of those skilled in the art regarding variations and implementations of the disclosed inventions, may be found in the following documents, all of which are hereby incorporated by reference:

Coburn, PLASMA ETCHING AND REACTIVE ION ETCHING (1982); HANDBOOK OF PLASMA PROCESSING TECHNOLOGY (ed. Rossnagel); PLASMA ETCHING (ed. Manos and Flamm 1989); PLASMA PROCESSING (ed. Dieleman et al. 1982); Schmitz, CVD OF TUNGSTEN AND TUNGSTEN SILICIDES FOR VLSI/ULSI APPLICATIONS (1992); METALLIZATION AND METAL-SEMICONDUCTOR INTERFACES (ed. Batra 1989); VLSI METALLIZATION: PHYSICS AND TECHNOLOGIES (ed. Shenai 1991); Murarka, METALLIZATION THEORY AND PRACTICE FOR VLSI AND ULSI (1993); HANDBOOK OF MULTILEVEL METALLIZATION FOR INTEGRATED CIRCUITS (ed. Wilson et al. 1993); Rao, MULTILEVEL INTERCONNECT TECHNOLOGY (1993); CHEMICAL VAPOR DEPOSITION (ed. M.L.Hitchman 1993); and the semiannual conference proceedings of the Electrochemical Society on plasma processing; Current Progess in Epitaxial Layer Transfer, Sakaguchi, et al., IEICE Transactions, Vol. E80-C, No.3, March 1997; Epitaxial Layer Transfer by Bond and Etchback of Porous Silicon, Yonehara, et al., Appl. Phys. Lett. 64 (16), 18 April 1994.